

FIG.1A

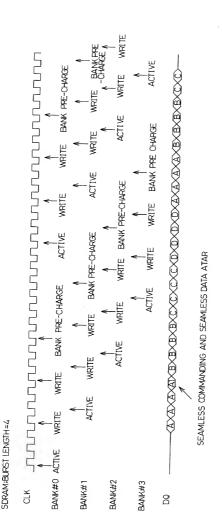


FIG.1B

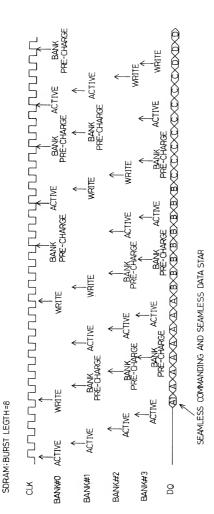
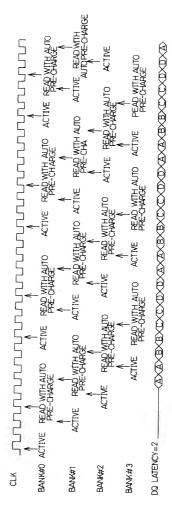


FIG.10

# SDRAM;LATENCY=2;BURST LENGTH=2;



F1G.2A

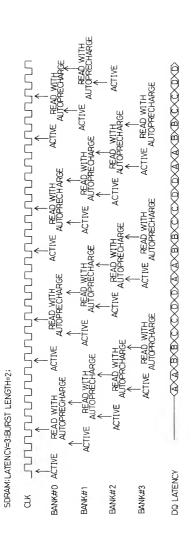
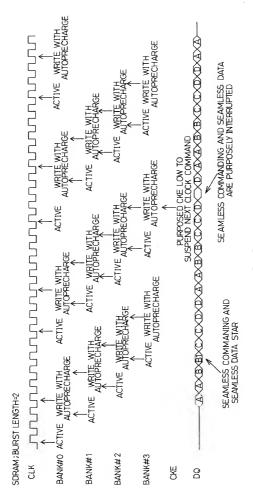


FIG. 2B



F16.2C

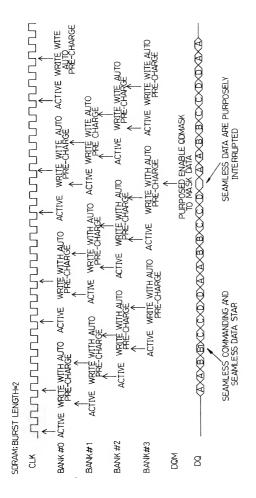


FIG.2D

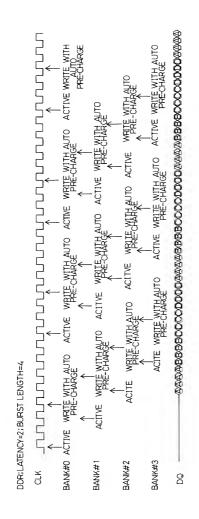


FIG.3A

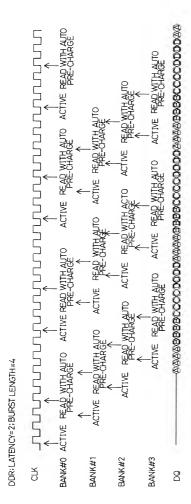


FIG.3B

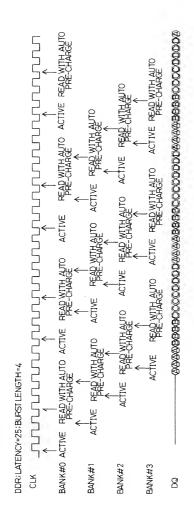


FIG.3C

RDRAM: TRR=8 TCYCLE; TCWD=6 TCYCLE; TRTP-4 TCYCLE;

ROWS (ACT ad)[[[[[]]]]ACT ED][[[[]]][[ACT co][[]][[]][[ACT co][PRER]]ACT eO][PRER]ACT EO][PRER]A -SEAMLESS ROW PACKET COMMANDING→

COG- [[][[][[][][][][][][WR allwr allwr allwerdwerei wer chercher chercher chercher allwereiner allwer SEAMLESS COL PACKET COMMANDING ---

-SEAMLESS L.O. DATA PACKET----

FIG.4A

TRANSACTION A:	a0 = {Da,Ba,Ra0}	a1={Da,Ba,Ca1}	a2={Da,Ba,Ca2}	TRANSACTION A: a0=(Da,Ba,Pa0) a1=(Da,Ba,Ca1) a2=(Da,Ba,Ca2) a3=(Da,Ba,Ca3) a4=(Da,Ba,Ca4)	a4= {Da,Ba,Ca4}
TRANSACTION B:	b0={Db,Bb,Rb0}	b1 = {Db,Bb,Cb1}	b2={Db,Bb,Cb2}	TRANSACTION B: b0={Db,Bb,Bb,Bb,Cb} bi={Db,Bb,Cb} bb,Cb} b5={Db,Bb,Cb} b3={Db,Bb,Cb} b5={Db,Bb,Cb}	b4 = {Db,Bb,Cb4}
TRANSACTION C:	c0={Dc,Bc,Rc0}	c1 = {Dc,Bc,Cc1}	c2={Dc,Bc,Cc2}	TRANSACTION C: c0={Dc,Bc,Rc0} c1={Dc,Bc,Cc1} c2={Dc,Bc,Cc2} c3={Dc,Bc,Cc3} c4={Dc,Bc,Cc4}	c4={Dc,Bc,Cc4}
TRANSACTION D: d0={Da,Ba,Rd0} d1={Da,Ba,Cd1} d2={Da,Bd,Cd2} d3={Dd,Bd,Cd3} d4={Dd,Bd,Gd4}	40={Da,Ba,Rd0}	d1 = {Dd,Bd,Cd1}	d2 ={Dd,Bd,Cd2}	{gpy'pg'pg}= gp	d4={Dd,Bd,Gd4}
TRANSACTION E:	e0={De,Be,Re0}	el ={De,Be,Ce1}	e2={De,Be,Ce2}	TRANSACTION E: e0=(De, Be, Pe0) e1={De, Be, Ce1} e2={De, Be, Ce2} e3={De, Be, Ce3} e4={De, Be, Ce4}	e4 ={De,Be,Ce4}

RDRAM:TRR=8 TCYCLE:TCAC=8 TCYCLE:TRAS=20 TCYCLE:TRDP=4 TCYCLE:

ROWS (par ad)[[[[[[par to]][[[par to]][[par to]] par to]] par to] par political par to] par par to] par to] SEAMLESS ROW PACKET COMMANDING→

රටුරු (()()()()()()()()()()()() ක ක්) න ක්දැන භ්ලා භ්ලා පෙලා යා අත යටු ක ක්ලා ක්රීත ක්රීත ක්රීත ප්රත යටු -SEAMLESS COL PACKET COMMANDING----

SEAMLESS L.O. DATA PACKET-

### FIG.4B

SDRAM:BURST LENGTH=4

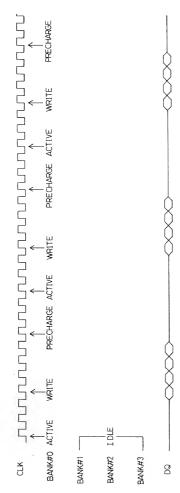


FIG.5 PRIORART

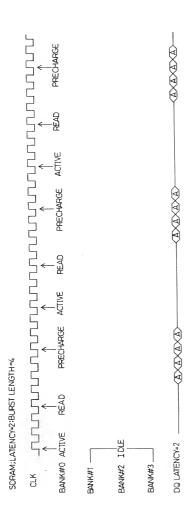


FIG.6A PRIOR ART

### SDRAM;LATENCY=3;BURST LENGTH=4

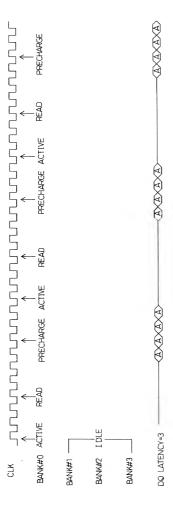
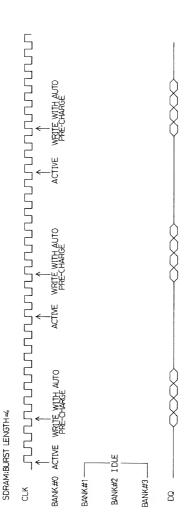


FIG.6B PRIOR ART



F1G.7 PRIOR ART



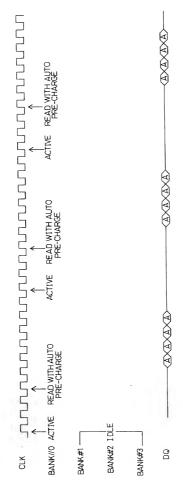
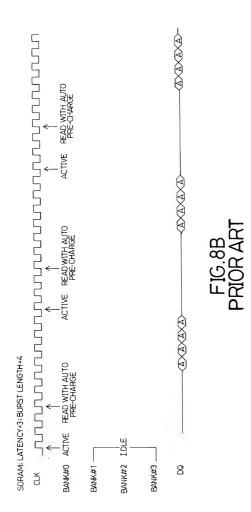


FIG.8A PRIOR ART



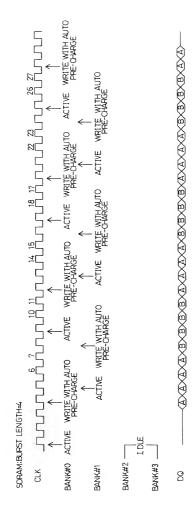
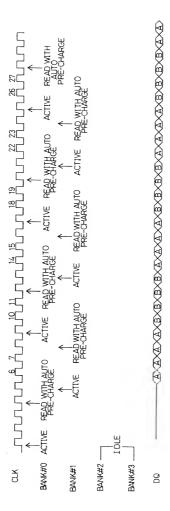


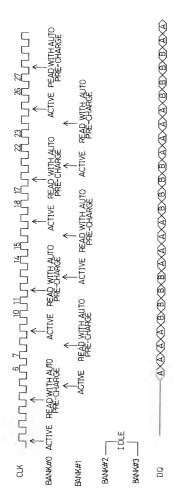
FIG.9 PRIOR ART

SORAM:LATENCY=2;BURST LENGTH=4



#### FIG.10A PRIOR ART

## SDRAM:LATENCY=3: BURST LENGTH=4



#### FIG.10B PRIOR ART

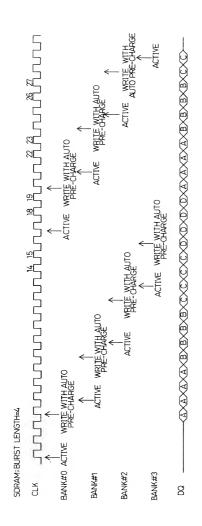


FIG.11 PRIOR ART

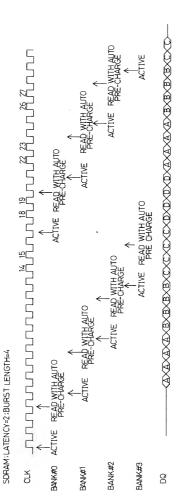


FIG.12A PRIOR ART

SDRAM;LATENCY=3;BURST LENGTH=4

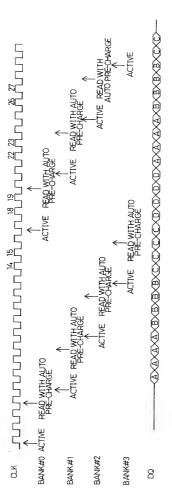


FIG.12B PRIORART